Taeyoung Kim

Ph.D
Staff AI Software Architect at Intel Corporation
Santa Clara, CA 95054

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Areas of interest

[12+ years] Software Engineering: Software Engineering for Machine Learning, Performance/Power Optimization, On-device Overclocking Optimization, Workload Characterization, EDA/CAD tool development (Expert on C++, C# , Python, Java, Perl, Matlab, SQL Databases, and Git) and Secure Development Life-cycle

[8+ years] System Modeling and Thermal/Reliability Simulation: System-level architectural modeling and simulation, system design flow and methods, reliability analysis, thermal simulation for SOC/platform.

[4 years] High-Speed I/O Simulation: I/O architecture, system-level modeling, simulation, and optimization. Platform-level channel simulation design for PCIe 3/4/5/6, Thunderbolt, USB3, Type C, UPI/QPI chip-to-chip interconnect, jitter decomposition analysis for high-speed I/O

[7 years] Real-time/Embedded/Firmware/FPGA System Design and Modeling: Embedded HW/SW design, Firmware Design for MCUs, FPGA HW/SW co-design and co-optimization

Experience

Staff AI Software Architect at AI Team,
Client Ecosystem Development Division,
Client Computing Group,
Intel Corporation, Santa Clara, CA, USA Jun.2021–Present

Senior Software Engineer at EDA/CAD Team,
Cores & Client CAD Division,
Design Engineering Group,
Intel Corporation, Hillsboro, OR, USA Jun.2017–Jun.2021

Software Intern Graduate Level at Signal & Power Integrity, System Modeling Group,
Design Technology Solutions,
Intel Corporation, Hillsboro, OR, USA Jun-Sep, 2016

Research Assistant, VLSI/FPGA/Real-time Embedded Systems,
Department of Computer Science and Engineering, University of California, Riverside, CA, USA, Sep.2013–Jun.2017

Research Staff, Full-time Research Staff, Real-time Embedded Systems, Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, USA, Jun.2012–Feb.2013

Research Assistant, Real-time/Embedded/Firmware Systems Design for MCUs, Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, USA, Jan.2010–May.2012

Lecturer, Part-time Instructor, Programming Language and Computer Security Classes, Kyungmin College, Uijeongbu, Korea, Aug.2007–May.2008

Research Assistant, Embedded/Firmware Systems Design for MCUs, Department of Electronics and Computer Engineering, Korea University, Seoul, Korea, Mar.2005–Feb.2008

Software Engineer Manager, eStop, Inc., Seoul, Korea, May.2004–Feb.2005

Software Engineer, Assistant Manager, System Software Engineering, Netpia, Inc., Seoul, Korea, Nov.2001–Apr.2004

Software Engineer, Staff, System Software Engineering, eStop, Inc., Seoul, Korea, Aug.1999–Apr.2000

Education

Ph.D. Computer Science, University of California, Riverside, CA, USA
Advisor: Dr. Sheldon X.-D. Tan GPA: 3.87/4.0
Sep.2013–June 16th 2017

M.S. Electrical Engineering, University of Virginia, Charlottesville, VA, USA
Aug.2009–May 20th 2012

M.Eng. Electronics and Computer Engineering, Korea University, Seoul, Korea
Mar.2005–Feb 24th 2007

B.S. Electronics Engineering, Konkuk University, Seoul, Korea
Mar.1997–Feb 22nd 2005

Honors and Awards

[2023/Q4] AI-based Overclocking Solution, Divisional Recognition Award (DRA), Client Ecosystem Development Recognition Award

[2023/Q4] AI-based Overclocking Solution, Divisional Recognition Award (DRA), Platform Software Engineering Recognition Award

[2016] Dissertation Year Program (DYP) Fellowship Award, University of California, Riverside

[2016] Finalist at ACM student Research Competition (SRC), ICCAD, Nov.

[2014, 2015, 2016] Travel Grant Award at ACM Student Research Competition (SRC), ICCAD, Nov.

[2016] Travel Grant Award at Young Faculty Workshop, Design Automation Conference (DAC), Jun.

[2015] Best Poster Research Award at ACM PhD Forum, Design Automation Conference (DAC), Jun.

[2015] Travel Grant Award at ACM PhD Forum, Design Automation Conference (DAC), Jun.

[2014] Richard Newton Fellowship Award, DAC, Jun.

[2013-2015] Dean's Distinguished Fellowship Award, University of California, Riverside.

[2013] In Recognition of Exceptional Presentation (2nd place), KSEA Virginia Regional Conference.

[2007] Outstanding Academic Performance Award, Korea University.

Professional Activities

[2017-Present], Associate Editor, AI/ML/System Integration, the VLSI Journal, ELSEVIER

[2023-Present], Technical Program Committee (TPC), AI/ML Track, Design, Automation and Test in Europe Conference (DATE)

[2022-Present], Technical Program Committee (TPC), AI/ML Track, Design Automation Conference (DAC)

[2021-Present], Technical Program Committee (TPC), AI/ML Track, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)

[2021-Present], Program Committee, Young Excellence (WYE) Program at IEEE Solid-State Circuits Society (ISSCC), IEEE

[2022], AI Track Session Chair, Asia and South Pacific Design Automation Conference (ASP-DAC)

[2020-2022], Standard Committee, IEEE P1924.1 Standard Working Group, Energy Efficient Comm Hardware, IEEE

[2017-2018], Program Committee, ACM Student Research Competition at International Conference On Computer Aided Design (ICCAD)

[2019-Present], Reviewer, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

[2018-Present], Reviewer, Microelectronics Journal, ELSEVIER

[2018-Present], Reviewer, Microelectronics Reliability Journal, ELSEVIER

[2018-Present], Reviewer, ACM Journal on Emerging Technologies in Computing Systems (JETC)

[2017-Present], Reviewer, ACM Transactions on Embedded Computing Systems (TECS)

[2016-Present], Reviewer, ACM Transactions on Design Automation of Electronic Systems (TODAES)

[2015-Present], Reviewer, IEEE Transactions On Very Large Scale Integration (VLSI) Systems (TVLSI)

Patents

System and Method on AI-based Overclocking (AIOC), Patent pending

Methods and apparatus to perform cloud-based artificial intelligence overclocking, Patent pending

Methods and apparatus to adapt memory channel usage on a per-user basis, US20220188016A1, Jun. 16, 2022 Accessed: Oct. 04, 2023.

Publications

Books

S. Tan, M. Tahoori, **T. Kim**, S. Wang, Z. Sun, and S. Kiamehr, Long-Term Reliability of Nanometer VLSI Systems: Modeling, Analysis and Optimization, 1st ed. Springer International Publishing, 2019. (Co-authored, 40% contribution)

Theses

T. Kim, *System-Level Electromigration-Induced Dynamic Reliability Management,* Ph.D. thesis University of California, Riverside, June, 2017

T. Kim, *Detection and Prevention of Forward Head Posture with Body Sensor Networks,* M.S. thesis University of Virginia, Charlottesville, May, 2012

T. Kim, *A Large Scale Indoor Localization System Based on Wireless Sensor Networks,* M.Eng. thesis, Korea University, Seoul, Feb, 2007

Journal Articles

[VLSIJ'18] **T. Kim**, S. X.-D. Tan, C. Cook, and Z. Sun, "Detection of Counterfeited ICs Via On-Chip Sensor and Post-Fabrication Authentication Policy", *Integration, the VLSI Journal*, vol. 63, pp. 31-40, Sep. 2018.

[MJ'18] **T. Kim**, Z. Liu, and S. X.-D. Tan, "Dynamic reliability management based on resource-based EM modeling for multi-core microprocessors," *Microelectronics Journal*, vol. 74, pp. 106-115, Apr. 2018.

[TVLSI'18] S. Wang, **T. Kim**, Z. Sun, S. X.-D. Tan, and M. B. Tahoori, "Recovery-Aware Proactive TSV Repair for Electromigration Lifetime Enhancement in 3-D ICs" *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 26, no. 3, pp. 531–543, Mar. 2018.

[TVLSI'18] S. Peng, H. Zhou, **T. Kim**, H. Chen, S. X.-D. Tan, "Physics-based Compact TDDB Models for Low-k BEOL Copper Interconnects with Time-Varying Voltage Stressing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)*, vol. 26, no. 2, pp. 239–248, Feb. 2018

[VLSIJ'18'] S. X.-D. Tan, H. Amrouch, **T. Kim**, Z. Sun, C. Cook, and J. Henkel, "Recent Advances in EM and BTI induced Reliability Modeling, Analysis and Optimization," *Integration, the VLSI Journal*, vol. 60, pp. 132–152, Jan. 2018.

[TDMR17] H. Chen, S. X.-D. Tan, **T. Kim**, and J. Chen, "Analytical Modeling of Electromigration Failure for VLSI Interconnect Tree Considering Temperature and Segment Length Effects," *IEEE Transactions on Device and Materials Reliability (TDMR)*, vol. 17, no. 4, pp. 653-666, Dec. 2017.

[VLSIJ'17] X. Huang, V. Sukharev, **T. Kim**, and S. X.-D. Tan, "Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing," *Integration, the VLSI Journal*, *Integration, the VLSI Journal*, vol. 58, pp. 518–527, Jun. 2017.

[TVLSI'17] **T. Kim**, Z. Sun, H. Chen, H. Wang, and S. X.-D. Tan, "Energy and Lifetime Optimizations for Dark Silicon Manycore Microprocessor Considering both Hard and Soft Errors", *IEEE Trans Very Large Scale Integration (VLSI) Systems (TVLSI)*, vol. 25, no. 9, pp. 2561-2574, Sep. 2017.

[TCAD'16] H. B. Chen, S. X.-D. Tan, X. Huang, **T. Kim** and V. Sukharev, "Analytical Modeling and Characterization of Electromigration Effects for Multibranch Interconnect Trees," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 11, pp. 1811-1824, Nov. 2016.

[VLSIJ'16] X. Huang, V. Sukharev, J.-H. Choy, M. Chew, **T. Kim**, S. X.-D. Tan, "Electromigration assessment for power grid networks considering temperature and thermal stress effects," *Integration, the VLSI Journal*, vol. 55, pp. 307–315, Sep. 2016

[TODAES'16] Z. Yue, **T. Kim**, H. Shin, S. X.-D. Tan, X. Li, H. Chen and H. Wang, "Statistical Rare Event Analysis and Parameter Guidance by Elite Learning Sample Selection", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 21, no. 4, p. 56:1–56:21, May 2016

[IJACCS'13] S. Chen, J. S. Brantley, **T. Kim**, S. A. Ridenour, and J. Lach, "Characterising and minimising sources of error in inertial body sensor networks," *Int. J. Auton. Adapt. Commun. Syst. (IJAACS)*, vol. 6, no. 3, pp. 253-271, May. 2013.

[WPC'12] W. Y. Lee, K. Hur, **T. Kim**, D. S. Eom, and J. O. Kim, "Large scale indoor localization system based on wireless sensor networks for ubiquitous computing," *Wireless Personal*, vol. 63, no. 1, pp. 241-260, Mar. 2012.

[TCE'08] D Eom, **T. Kim**, H. Jee, H. Lee and J. Han, "A Multi-Player Arcade Video Game Platform with A Wireless Tangible User Interface", *IEEE Transactions on Consumer Electronics*, , vol. 54, no. 4, pp. 1819–1824, Nov. 2008.

Conference Proceedings

[SMACD'19] Z. Sun, **T. Kim**, M. Chow, S. Peng, H. Zhou, H. Kim, D. Wong and S. X.-D. Tan, "Long-Term Reliability Management For Multitasking GPGPUs" *International Conference on Synthesis, Modeling Analysis and Simulation Methods and Applications to Circuit Design (SMACD2019)*, Lausanne, Switzerland, Jul. 2019.

[SMACAD'17] Y. Ye, **T. Kim**, S. X.-D. Tan, H. Chen and H. Wang, "Comprehensive Detection of Counterfeit ICs Via On-Chip Sensor and Post-Fabrication Authentication Policy," *International Conference on Synthesis, Modeling Analysis and Simulation Methods and Applications to Circuit Design (SMACD2017)*, Taormina, Italy, Jun. 2017.

[ICCAD'16] **T. Kim**, Z. Sun, C. Cook, J. Gaddipati, H. Wang, H. Chen, S. X.-D. Tan, "Dynamic Reliability Management for Near-Threshold Dark Silicon Processors", *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD2016)*, Austin, TX, Nov. 2016.

[ICCAD'16] Z. Sun, E. Demircan, M. D. Shroff, **T. Kim**, X. Huang and S. X.-D. Tan, "Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects", *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD2016)*, Austin, TX, Nov. 2016.

[SMACD'16] C. Cook, Z. Sun, **T. Kim** and S. X.-D. Tan, "Finite Difference Method for Electromigration Analysis of Multi-Branch Interconnects," *International Conference on Synthesis, Modeling Analysis and Simulation Methods and Applications to Circuit Design (SMACD2016)*, Lisbon, Portugal, Jun. 2016.

[DAC'16] **T. Kim**, Z. Sun, C. Cook, H. Zhao, R. Li, D. Wong, S. X.-D. Tan, "Cross-layer modeling and optimization for electromigration induced reliability", *Proc. IEEE/ACM Design Automation Conference (DAC2016)*, Austin, TX, June, 2016.

[DAC'16] X. Huang, V. Sukharev, Z. Qi, **T. Kim**, H. Chen, S. X.-D. Tan, "Physics-Based Full-Chip TDDB Assessment for BEOL Interconnects", *Proc. IEEE/ACM Design Automation Conference (DAC2016)*, Austin, TX, June, 2016.

[DATE'16] **T. Kim**, X. Huang, H. Chen, V. Sukharev, S. X.-D. Tan, "Learning-based Dynamic Reliability Management for Dark Silicon Processor Considering EM Effects", *Proc. Design, Automation and Test in Europe (DATE2016)*, Dresden, Germany, March 2016.

[ASPDAC'16] X. Huang, V. Sukharev, **T. Kim**, H. Chen, S. X.-D. Tan, "Electromigration Recovery Modeling and Analysis under Time-Dependent Current and Temperature Stressing", *Proc. Asia South Pacific Design Automation Conference (ASP-DAC2016)*, Macao, China, Jan. 2016.

[3DTEST'15] **T. Kim**, X. Huang, V. Sukharev and S. X.-D. Tan, "Learning-Based Reliability Management for Dark Silicon Systems", *Sixth IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (3D-TEST2015)*, Anaheim, CA, Oct, 2015.

[TECHCON'15] **T. Kim**, X. Huang, V. Sukharev, X. X.-D. Tan, "A Dynamic Reliability Management Framework for Dark Silicon", *TECHCON*, Austin, Sep, 2015.

[DAC'15] H. Chen, X. Huang, V. Sukharev, S. X.-D. Tan, **T. Kim**, " Interconnect reliability modeling and analysis for multi-branch interconnect trees," *Proc. IEEE/ACM Design Automation Conference (DAC2015)*, San Francisco, June, 2015.

[ICCAD'14] **T. Kim**, B. Zheng, H. Chen, Q. Zhu, V. Sukharev and S. X.-D. Tan, "Lifetime optimization for real-time embedded systems considering electromigration effects," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD2014)*, San Jose, CA, Nov. 2014

[DAC'14] T. Wei, **T. Kim**, S. Park, Q. Zhu, S. X.-D. Tan, N. Chang, S. Ula, M. Maasoumy, "Battery management and application for energy-efficient buildings," *Proc. IEEE/ACM Design Automation Conference (DAC2014)*, San Francisco, June, 2014

[BSN'11] **T. Kim**, S. Chen, J. Lach, "Detecting and Preventing Forward Head Posture with Wireless Inertial Body Sensor Networks," *International Conference on Body Sensor Networks (BSN2011)*, PP. 125-126, May, 2011

[WH'10] A.T. Barth, B.C. Bennett, B. Boudaoud, J.S. Brantley, S. Chen, C.L. Cunningham, **T. Kim**, H.C. Powell, Jr., S.A. Ridenour, J. Lach, "Longitudinal High-Fidelity Gait Analysis with Wireless Inertial Body Sensors," *IEEE Wireless Health Conference*, 192-3, Oct. 2010.

[BODYNET'10] S. Chen, J. S. Brantley, **T. Kim**, and J. Lach, "Characterizing and Minimizing Synchronization and Calibration Errors in Inertial Body Sensor Networks," in *Proceedings of the Fifth International Conference on Body Area Networks (BodyNet2010)*, Corfu, Greece, pp. 138-144. Sep. 2010.

Teaching

Teaching Assistant, University of California, Riverside
Winter, 2017 EE260 Advanced VLSI
Fall, 2016 EE213 Computer-Aided Electronic Circuit Simulation
Winter, 2016 CS168 Introduction to VLSI
Fall, 2014 CS100 Software Construction

Teaching Assistant, University of Virginia
Fall, 2011 ECE3660 Electronics II

Full Time Lecturer, Kyungmin College,
Spring, 2008, Internet Programming
Fall, 2007, Internet and Computer Security

Teaching Assistant, Korea University,
Spring, 2007 KEEE474 Embedded Software
FALL, 2006 KEEE491 Capstone Project Lab

Mentoring

Hsin-Yu Fan Chiang (UCR, undergrad) - Project: Content Management System for Research Archive

Zhenning Jiang (UCR, undergrad) - Project: FPGA Debug Analyzer

Hui Li (UCR, undergrad) - Project: FPGA Debug Analyzer

He Dai (UCR, undergrad) - Project: FPGA Debug Analyzer

Shawn Kim (UVA, undergrad) - Project: Posture Detection System

Jeremy Kim (UVA, undergrad) - Project: Posture Detection System

Hana Lee (Korea Univ, undergrad) - Project: Motion Detection-based Virtual Game

Heejin No (Korea Univ, undergrad) - Project: Motion Detection-based Virtual Game

Graduate Classes

UCR-CS210-Scientific Computing: Grade A+

UCR-CS220-Synthesis of Digital System: Grade A+

UCR-CS229-Machine Learning: Grade A+

UCR-EE260-Embedded Real-time Systems: Grade A+

UCR-EE213-Computer Aided Electrical Circuit Simulation: Grade A

UCR-CS223-Reconfigurable Computing-FPGA Architecture: Grade A

UCR-CS201-Compiler Construction: Grade A

UCR-CS217-GPU Architecture Parallel Programming: Grade A

UCR-CS211-High Performance Computing: Grade A

UCR-CS203A-Computer Architecture

UCR-CS238-Algorithm Technique Computational Biology

UVA-ECE6332-VLSI

UVA-ECE5750-Digital Signal Processing

Professional Membership

2017-Present, Professional Member, Association for Computing Machinery (ACM)

2014-2017, Student Member, Association for Computing Machinery (ACM)

2017-Present, Professional Member, ACM Special Interest Group on Design Automation (SIGDA)

2014-2017, Student Member, ACM Special Interest Group on Design Automation (SIGDA)

2017-Present, Member, Institute of Electrical and Electronics Engineers (IEEE)

2010-2017, Student Member, Institute of Electrical and Electronics Engineers (IEEE)